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Performance improvement of solution-processed CdS/CdTe solar cells with a thin compact TiO_2 buffer layer

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Abstract The device performance of CdS/CdTe solar cells largely depends on not only the back ohmic contact, but also the conformality of CdS window layer coating. In order to reduce the light absorption loss in CdS, the CdS thickness is usually less than 100 nm. However, pinholes in CdS and non-conformal coverage of CdS on transparent conducting oxide layer will cause shunting thus leading to device performance degradation and failure. In this paper, low-temperature and low-cost fabrication methods, i.e., chemical bath deposition and electrochemical deposition, were used to deposit CdS and CdTe, respectively. It was found that the yield of device was around 20 % due to shunting. In order to alleviate this problem, a compact layer of TiO_2 was inserted between the fluorine-doped tin oxide and CdS as a buffer layer. The thickness effect of TiO_2 was studied and showed that devices with thin (20 nm thickness) TiO_2 performed better than the counterparts with thick layers. It was discovered that device yield improved to 80 % and stability in air substantially improved with TiO_2 layer.

Keywords Thin films · Titanium dioxide · Solar energy · Cadmium compounds

1 Introduction

Polycrystalline cadmium sulfide/cadmium telluride (CdS/CdTe) is one of the most important thin-film photovoltaic material systems. In 2014, a certified 21.5 % power conversion efficiency was achieved by First Solar, Inc., on CdTe solar cell, which is close to the highest single-junction thin-film solar cell efficiency 21.7 % of copper–indium–gallium–selenide (CIGS) [1–3]. As a binary compound, CdTe films can be deposited with a much simpler and reproducible process as compared with CIGS. These facts together suggest the ongoing potential of CdTe thin-film photovoltaic technology. Currently, the mainstream CdTe deposition methods require a high-temperature process and vacuum equipment [4–8]. In this work, solution-based electrochemical deposition (ED) method was adopted to fabricate CdTe films due to its low deposition temperature (<100 °C) which not only reduces the fabrication cost but also makes it suitable for future flexible and/or nanostructured photovoltaic devices. For the conventional superstrate device configuration, namely, glass/TCO (transparent conducting oxide)/CdS/CdTe/ back contact, much effort has been devoted to exploration of ohmic back contact to the p-type CdTe [9–13]. Nevertheless, attention must also be paid to addressing shunting problem caused by pinholes in CdS or incomplete coverage of CdS on TCO, which significantly affects device yield and reliability. Generally, there are two solutions to this problem: (1) using a high-resistivity transparent oxide together with low-resistivity TCO, e.g., undoped tin oxide (TO) or ZnO with fluorine-doped tin oxide (FTO) and (2) using a thick

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CdS layer for complete conformal coverage of TCO which will increase unfavorable light absorption losses in CdS layer [14–16]. Thick CdS layer also causes major current loss due to parasitic light absorption which adversely affects fill factor (FF). High resistive transparent (HRT) buffer layers are explored in the past using ZnO as HRT between TCO and CdS. Thickness effect of ZnO is explored and found HRT ZnO layer improved the device performance of CdTe solar cells by overcoming non-uniformity issues in CdS layer [17, 18]. ZnO has instability problem in humid environment leading to low power conversion efficiency [19]. This work presents the use of TiO_2 as a buffer layer between CdS and TCO to avoid issues with thick CdS layer and pinholes problem using thin CdS. Effect of TiO_2 thickness on device yield and stability in open air is also explored. In this work, CdS and CdTe were deposited by low-cost solution processes: chemical bath deposition (CBD) and ED, respectively. In experiments, 6.1 % efficiency was achieved from the FTO/CdS/CdTe/Au solar cell without any back contact optimization. A compact TiO_2 layer as the buffer layer was utilized to address shunting issues and improve CdTe/CdS photovoltaic device yield and reliability. The role of TiO_2 in CdTe/CdS solar cell and thickness effect of TiO_2 were carefully studied. It was found that by using a TiO_2 layer with optimal thickness, the device yield was significantly improved from around 20 % to around 80 %, with a peak efficiency of 8.0 %. Devices without TiO_2 showed the problem of shunting resulting in low working devices (yield) per sample. A good solar cell should have optimum energy conversion ability without shunting issue. The device performance stability was also clearly improved. These results indicate that inserting a thin layer of TiO_2 can be a reliable solution to device shunting problems of CdS/CdTe solar cells.

2 Materials and methods

2.1 Substrate cleaning

The soda-lime glasses coated with 600-nm-thick FTO transparent conducting layer (Hartford Glass Co. Inc.) were cleaned in ultrasonic cleaner with detergent, acetone, isopropyl alcohol (IPA) and deionized water successively.

2.2 TiO_2 sputtering

TiO_2 was deposited using DC reactive magnetron sputtering method with the following conditions: The gas flow was 4 standard cubic centimeters per minute (sccm) O_2 mixed with 25 sccm Ar; the chamber pressure was 0.6 Pa; and the target was Ti metal (purity 99.9 %, China Rare Metal Material Co. Ltd.) circular in shape with diameter of 2 inch. DC sputtering power used was 200 W. Different deposition time was used to achieve different TiO_2 thicknesses ranging from 20 to 100 nm. TiO_2 thickness was measured during sputtering using quartz crystal thickness monitor installed inside sputtering chamber. After sputtering, TiO_2 samples were annealed in furnace at 500 °C for 30 mins with a gas flow of compressed air (300 sccm). Deposited TiO_2 was found amorphous in nature because sputtering method without heating the substrate was used to deposit TiO_2 layer. To convert TiO_2 to anatase, TiO_2 was annealed at 500 °C for 30 mins with a gas flow of compressed air (300 sccm). If it is annealed further or temperature is increased, TiO_2 will be converted to rutile phase which has lower photocatalyst activity as compared to anatase phase [20].

2.3 CdS chemical bath deposition (CBD)

CdS was deposited by CBD method at 90 °C for 30 min. The CBD solution was made by mixing 5×10^{-4} mol/L cadmium acetate ($Cd(CH_3COO)_2$), 5×10^{-4} mol/L thiourea (CH_4N_2S), 3×10^{-2} mol/L ammonium acetate ($Cd(CH_3COO)_2$) and 0.5 mol/L ammonium hydroxide (NH_4OH) [21–23].

2.4 CdTe electrochemical deposition

CdTe was deposited on the CdS layer using ED method. Temperature of ED bath was set at 85 °C. The three-electrode system was adopted for deposition with the carbon rod and the Ag/AgCl electrode serving as working electrode, counter electrode and reference electrode, respectively. The −610 mV potential versus Ag/AgCl was provided by the potentiostat CHI1000C. The solution was prepared by mixing pH 1.8 sulfuric acid (H_2SO_4), 0.7 mol/L cadmium sulfate ($CdSO_4$), 3.56×10^{-3} mol/L cadmium chloride ($CdCl_2$) and tellurium dioxide (TeO_2) [24, 25].

2.5 $CdCl_2$ treatment

After CdTe deposition, the samples were rinsed with deionized water and then soaked in oversaturated $CdCl_2$ methanol solution at 60 °C for 20 min, followed by rinsing with methanol and blow dry with compressed air. Then, the samples were annealed at 370 °C for 5 min with a gas flow of Ar (200 sccm) and compressed air (200 sccm) [5, 6, 26]. It was found that longer annealing of CdTe or postannealing methanol rinsing caused peeling of CdTe layer from substrate.

2.6 Back contact fabrication

Finally, arrays of twelve 50-nm-thick Au dots (0.0314 cm^2) were deposited by thermal evaporation.

2.7 Efficiency measurement

The power conversion efficiency was measured with the solar simulator (Newport Corporation, 91150 V) under an AM1.5 spectrum at one sun (1,000 W/m^2) illumination. Copper wires were connected with Au back contact using Ag paste for efficiency measurement.

3 Results and discussion

The fabricated device structure is shown in Fig. 1a, and a device photograph is shown in Fig. 1b. This is the conventional superstrate structure, in which light comes through the glass. The p-type CdTe and n-type CdS form a heterojunction with light absorbed mainly in CdTe layer. In order to determine the thicknesses of each layer, a cross-sectional scanning electron microscope (SEM) image was taken and is shown in Fig. 1c. In this image, it can be resolved that CdS layer is less than 100 nm thick and CdTe thickness is around 1.1 μm. The TiO_2 thickness in our experiments varied from 20 to 100 nm. In Fig. 1d, the band diagram of the FTO/TiO_2/CdS/CdTe/Au is illustrated [27, 28]. In principle, if CdS layer is pinhole free, it can block the photogenerated holes in CdTe layer. Due to thin CdS layer, pinholes are inevitable, especially in the cases where thin CdS layer is deposited for less light absorption loss. In these cases, the TiO_2 layer can not only provide a smooth transition for electrons but also help to block the holes when CdS layer is absent at the FTO surface. TiO_2 in perovskite solar cells also helps in improving efficiency by stopping holes from going to TCO front contact [29]. This implies TiO_2 window layer also helps in the separation of charge carriers and reduces the recombination rate.

In order to identify the optimum thickness for TiO_2, solar cell devices with 20-, 40-, 60-, 80- and 100-nm-thick TiO_2 were fabricated and their efficiencies were measured. Devices without TiO_2 (0-nm TiO_2) were also fabricated and used as reference cells. Figure 2a shows the current density–voltage (J–V) curves of the representative devices. And Fig. 2b–d shows peak and average device efficiencies, short-circuit current densities, open-circuit voltages, and FFs for each TiO_2 thickness group with statistic error bars. It can be seen from Fig. 2b that the peak efficiency for the devices without TiO_2 layer is 6.1 %, and the peak efficiency for the devices with 20 nm TiO_2 is 8.0 %. Device efficiencies of 40-, 60-, 80- and 100-nm-thick TiO_2 cells are all decreased compared with the reference cell. In Fig. 2c, short-circuit current density (J_{SC}) decreases with the increase in TiO_2 thickness, which is caused by possible reason: poor carrier transport through thick TiO_2 layer because of low mobility in TiO_2 layer [19] which decreases the collection of electrons at front contact. Another reason is that with the increase in the thickness of the film, the built-in electric field intensity distribution is significantly affected. The photogenerated charge carriers will not be effectively collected, so all the solar cell characteristics decreased with the increase in film thickness [17]. It implies thick TiO_2 reduces mobility and increases series

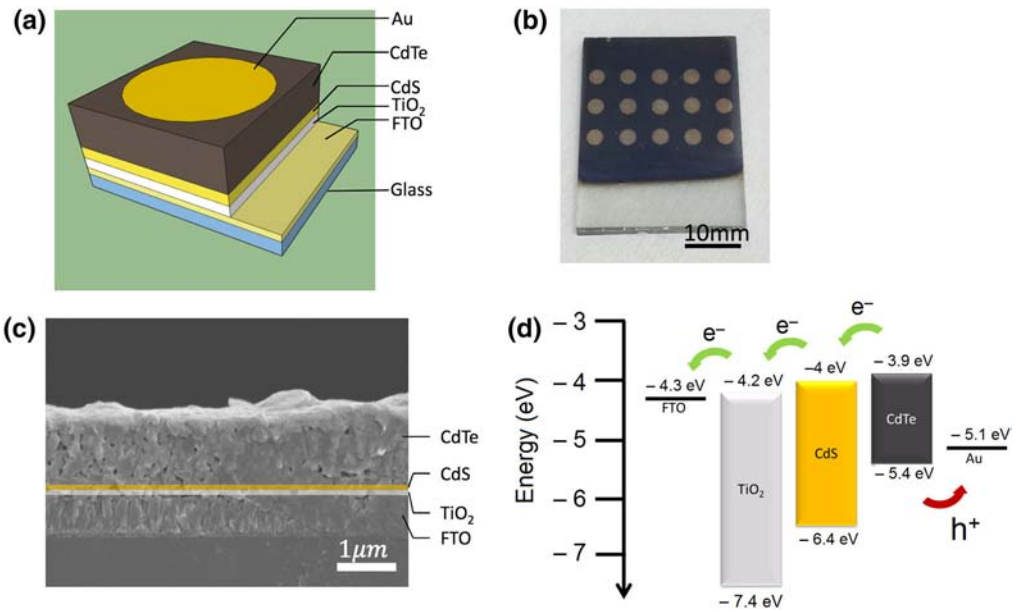

Fig. 1 (Color online) **a** Diagram of the CdTe/CdS solar cell device. **b** Photograph of the complete device. **c** Cross-sectional SEM image of the CdTe/CdS solar cell device. **d** Band energy diagram of the CdTe/CdS solar cell device

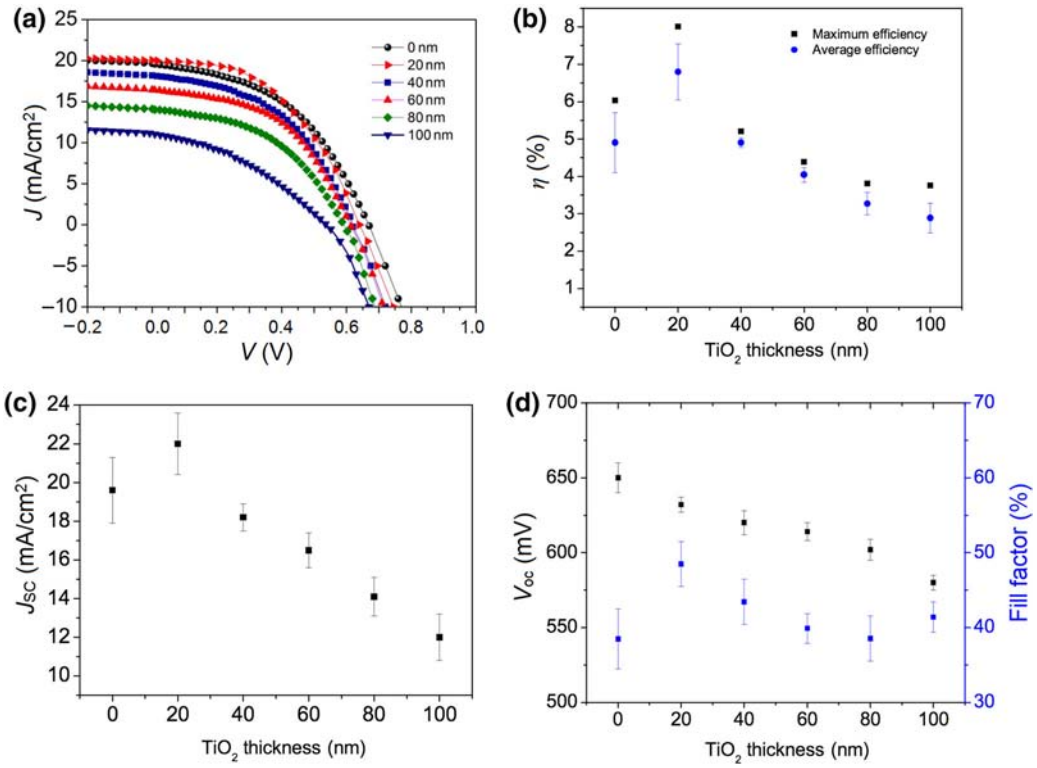

Fig. 2 (Color online) **a** *J–V* curves, **b** short-circuit current densities, **c** fill factors and **d** open-circuit voltages of CdTe/CdS solar cells with different TiO_2 buffer layer thicknesses (varied from 0 to 100 nm)

resistivity of TiO_2, reducing J_{SC} and FF. Intriguingly, the J_{SC} with 20-nm-thick TiO_2 is much higher than that of without TiO_2, which indicates that a very thin layer of TiO_2 will improve the photocurrent output. In Fig. 2d, open-circuit voltage (*Voc*) and FFs are demonstrated. It can be seen that the overall trend is that *Voc* drops with increasing TiO_2 thickness, and FF slightly increases with the increase in TiO_2 thickness and then degrades with over 60-nm TiO_2 thickness. These observations suggest that although thin TiO_2 layer improves device performance, excessive thickness degrades the performance of the device.

The materials were characterized by both SEM and X-ray diffraction (XRD), and the data are shown in Fig. 3. The SEM image in Fig. 3a is the surface morphology of the CdTe after $CdCl_2$ treatment and annealing at 370 °C for 5 min. The grain size of CdTe is less than 500 nm as measured through SEM. And XRD image in Fig. 3a shows that the electrochemically deposited CdTe is polycrystalline with preference orientation in (111). Data from XRD plot show that CdTe structure is highly (111) oriented. Figure 3b, e are the surface SEM and the XRD spectrum of chemical bath-deposited CdS. Surface SEM of CdS is taken on glass substrate. XRD of CdS showed peaks at 27°, 44° and 52° which corresponds to (111), (220) and (311) planes of cubic CdS [30]. The SEM image in Fig. 3c illustrates that the TiO_2 layer deposited by DC reactive magnetron sputtering method is very compact and the diffraction peaks at 25° and 48° indicate the anatase phase of annealed TiO_2. XRD and SEM measurement for TiO_2 is taken on FTO glass. Diffraction peaks at 25° and 48° correspond to (101) and (200) peaks of anatase TiO_2, respectively, while other peaks are from FTO glass substrate.

During fabrication, device failures were very common for the FTO/CdS/CdTe/Au cells due to two possible reasons: (1) The CdS layer was too thin to provide a conformal coverage on FTO; thus, pinholes may appear; CdS layer cannot be made thick to avoid light loss in CdS. It was observed thin CdS layer deposited by CBD showed pinholes on surface. (2) The solution-processed CdTe had fine grains (less than 500 nm) and inferior crystallinity which led to a lower mobility and a shorter collection length of photogenerated carriers [14, 31]. Therefore, TiO_2 layers of different thicknesses were added between FTO and CdS layers to overcome the short-circuiting problems brought by very thin CdS and the rough FTO surface. Note that thick CdS leads to excessive light loss; thus, thin CdS is usually preferred. The device yields (defined as the ratio of the number of working devices over the number of total devices) with different TiO_2 thicknesses are shown in

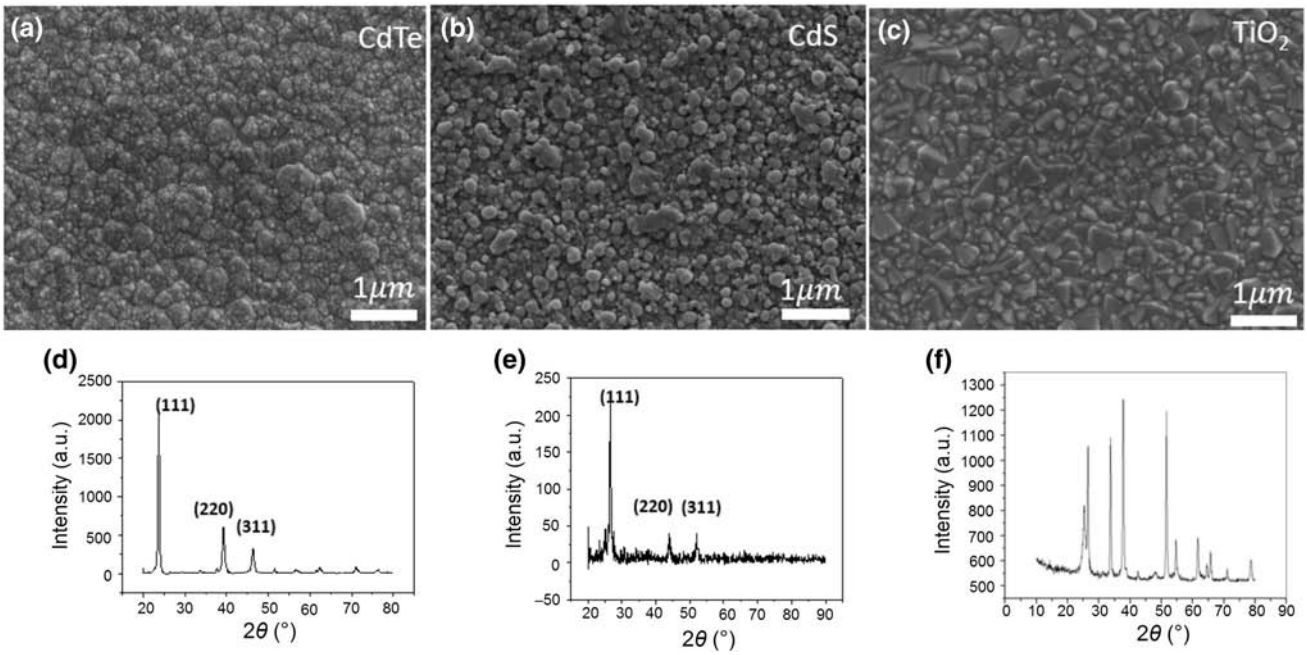

Fig. 3 SEM images of CdTe (**a**), CdS (**b**) and TiO_2 (**c**) surfaces. (**d**)–(**f**) are corresponding XRD patterns for each material. As for XRD in (**c**), diffraction peak at 25° corresponds to (101), diffraction peak at 48° corresponds to (200), and other peaks are from FTO glass

Fig. 4a. For the reference cell group, only around 20 % devices worked, whereas more than 80 % devices worked if a TiO_2 layer was added. The device improvement from TiO_2 is not only in device yield but also in device stability. The device degradation was measured and is shown in Fig. 4b. After being kept in air for two months, the efficiency of the reference cell devices dropped by 23 % (from 6.1 % to 4.7 %), whereas the efficiency of 20-nm TiO_2 devices with the same efficiency only dropped by 3 % (from 6.1 % to 5.9 %). Efficiency drop of most efficient cell with 20 nm was also recorded and was found to drop from 8.1 % to 7.6 %. This observation indicated that a compact TiO_2 layer was also helpful for improving the device stability in long term. Note that TiO_2 does not have the instability problem in humid environment as ZnO which was used in some work for the same purpose [32, 33]. Also, during stability measurements, the CdTe solar devices were not passivated. Therefore, even better stability is expected if the devices are well packaged following industrial standard.

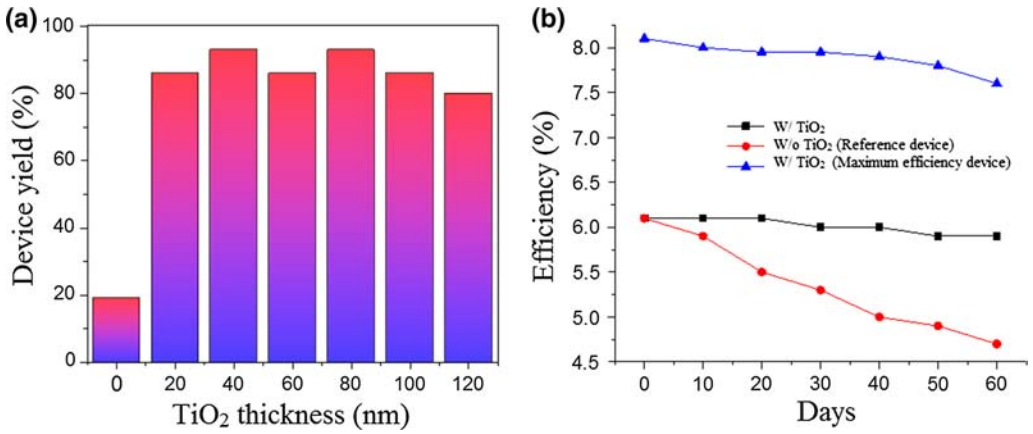

Fig. 4 (Color online) **a** Device yields with different TiO_2 thicknesses. **b** Efficiency degradation in air of the maximum efficiency cell (curve with triangles), reference cell (curve with dots) and the cell with 20-nm-thick TiO_2 (curve with squares)

4 Conclusions

In this work, thin-film polycrystalline CdTe/CdS solar cells were fabricated with solution processes. The reference cell with standard glass/FTO/CdS/CdTe/Au structure achieved 6.1 % maximum efficiency. However, the device yield was only 20 % which is too low for practical application. By inserting a compact TiO_2 layer with 20 nm thickness, device yield was improved to more than 80 % with a peak efficiency of 8.0 %. We observe that the compact TiO_2 buffer layer helps to solve the short-circuiting problems caused by thin non-uniform CdS. The addition of a compact TiO_2 layer was also found to significantly improve device stability. This study can further shed light on CdS/CdTe solar cell device failure mechanism and provide a viable solution to high-performance and high-yield devices.

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Conflict of interest The authors declare that they have no conflict of interest.

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